FIG. 1A

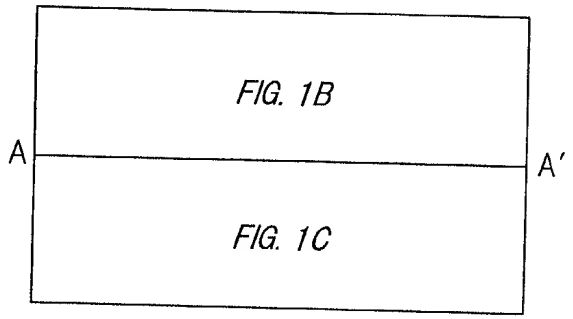

FIG. 1B

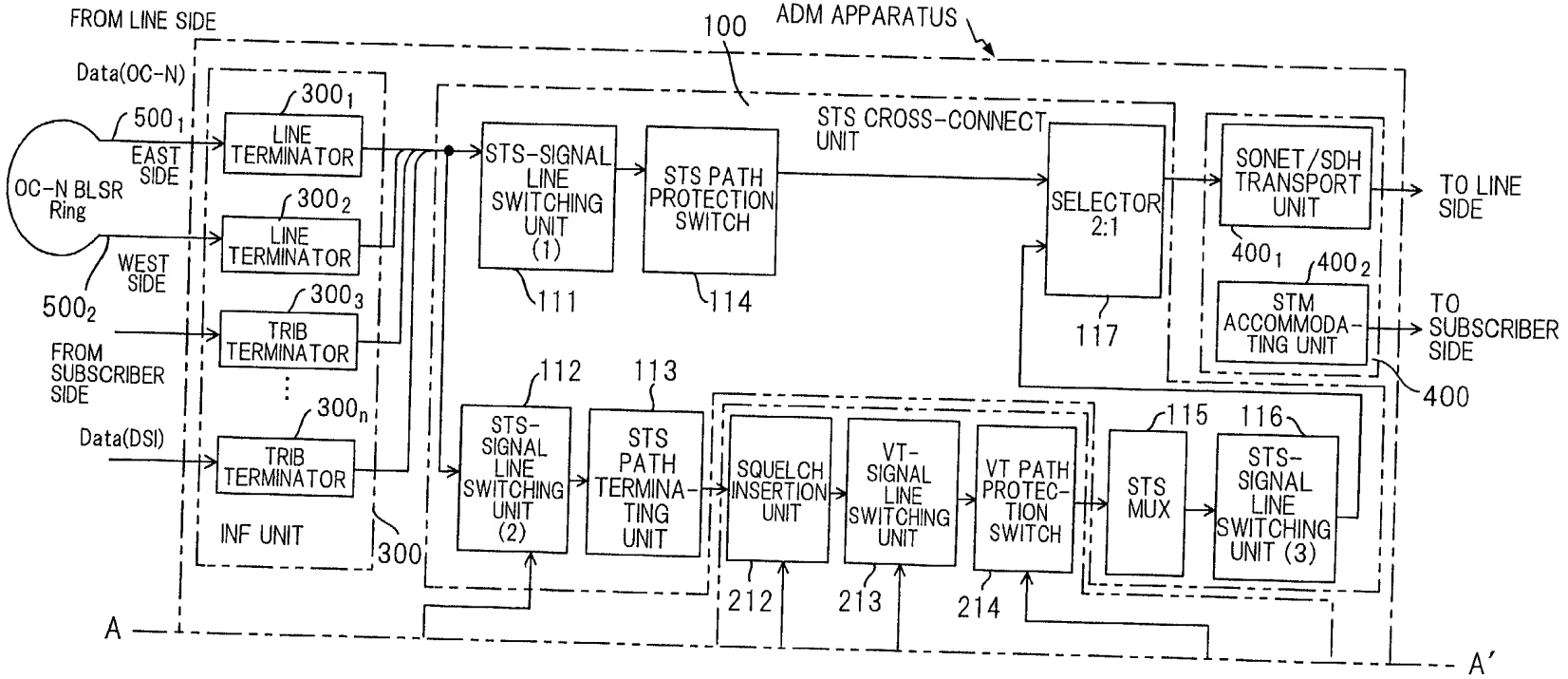

FIG. 1C

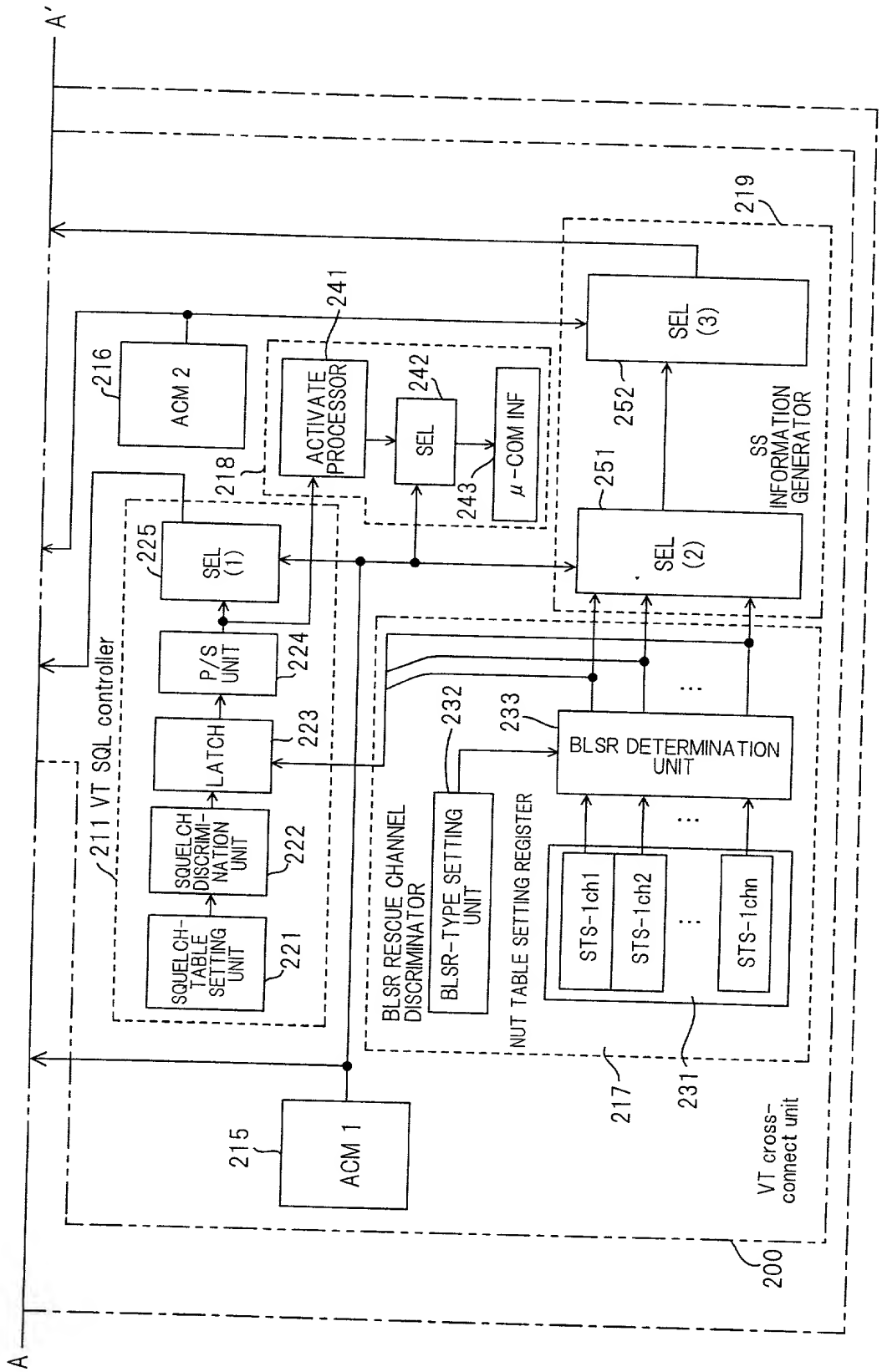
A
A'
200
VT cross-connect unit
215
ACM 1
216
ACM 2
217
231
NUT TABLE SETTING REGISTER
STS-1ch1
STS-1ch2
STS-1chn
BLSR RESCUE CHANNEL DISCRIMINATOR
BLSR-TYPE SETTING UNIT
232
233
BLSR DETERMINATION UNIT
211 VT SQL controller
SQUELCH-TABLE SETTING UNIT
221
SQUELCH DISCRIMI-NATION UNIT
222
LATCH
223
P/S UNIT
224
225
SEL (1)
218
ACTIVATE PROCESSOR
241
SEL
242
243
μ-COM INF
219
SEL (2)
251
SEL (3)
252
SS INFORMATION GENERATOR

FIG. 2

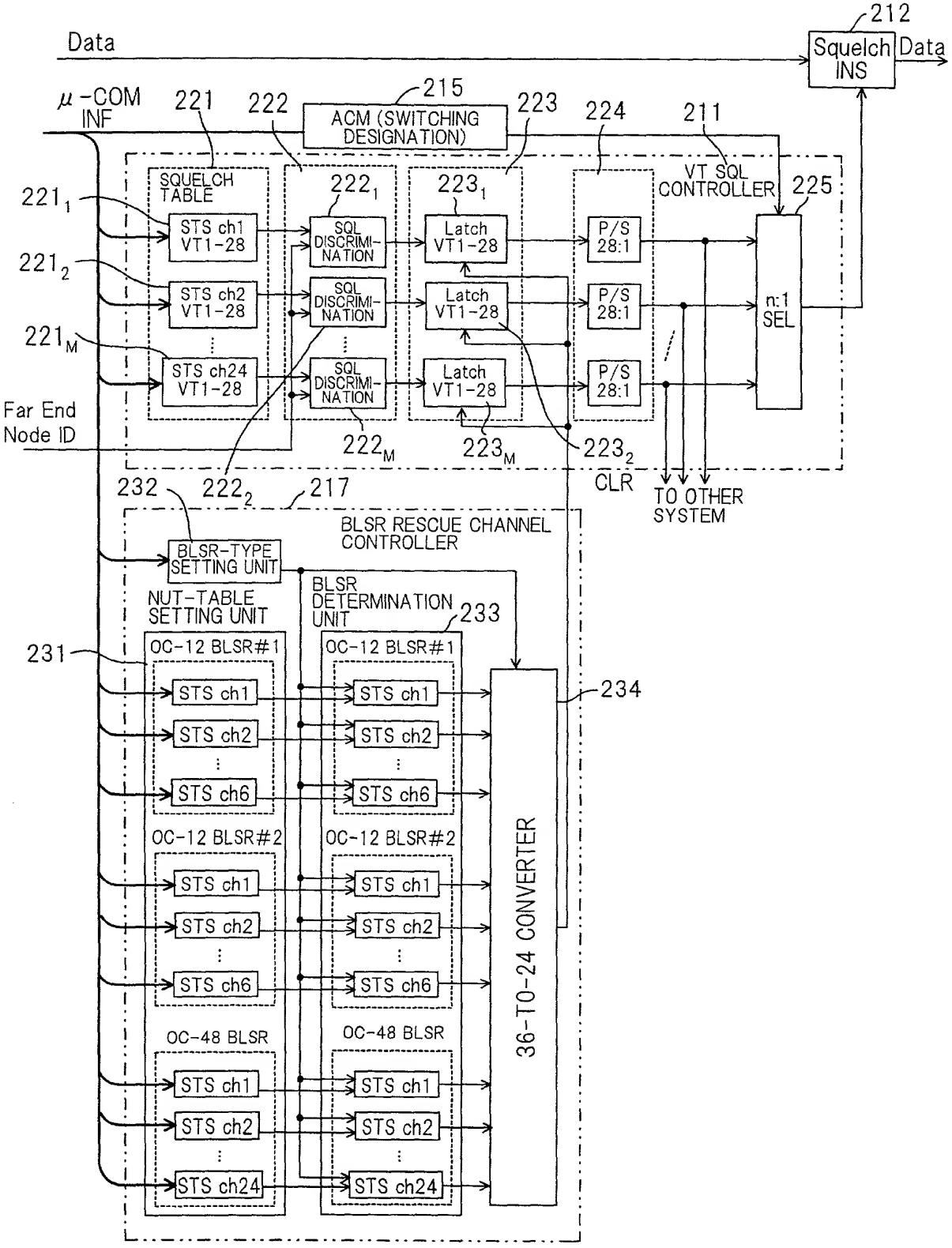
Data
212
Squelch INS
Data
μ-COM INF
221
222
215
ACM (SWITCHING DESIGNATION)
223
224
211
SQUELCH TABLE
VT SQL CONTROLLER
225
221 1
221 2
221 M
STS ch1 VT1-28
STS ch2 VT1-28
STS ch24 VT1-28
222 1
223 1
SQL DISCRIMI-NATION
Latch VT1-28
P/S 28:1
n:1 SEL
Far End Node ID
222 M
223 M
223 2
CLR
TO OTHER SYSTEM
232
222 2
217
BLSR RESCUE CHANNEL CONTROLLER
BLSR-TYPE SETTING UNIT
NUT-TABLE SETTING UNIT
BLSR DETERMINATION UNIT
233
231
OC-12 BLSR#1
OC-12 BLSR#2
OC-48 BLSR
STS ch1
STS ch2
STS ch6
STS ch24
234
36-TO-24 CONVERTER

FIG. 3A

<CONFIGURATION FOR
OC-12 BLSR APPLICATION>

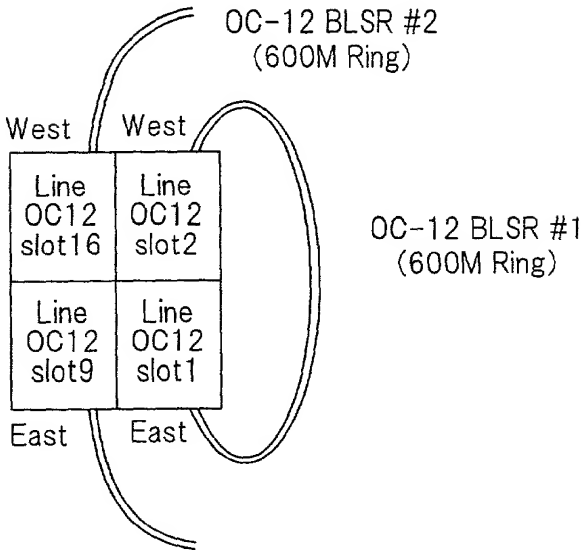

FIG. 3B

<CONFIGURATION FOR
OC-48 BLSR APPLICATION>

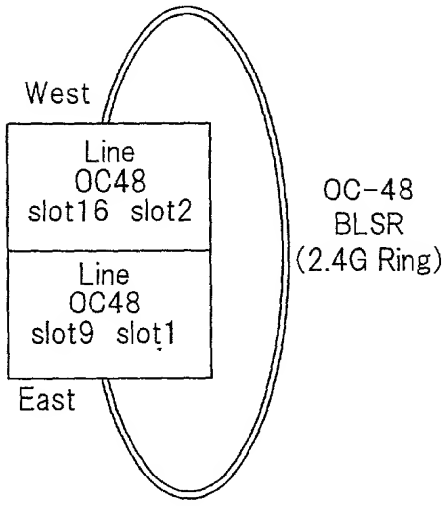

FIG. 4

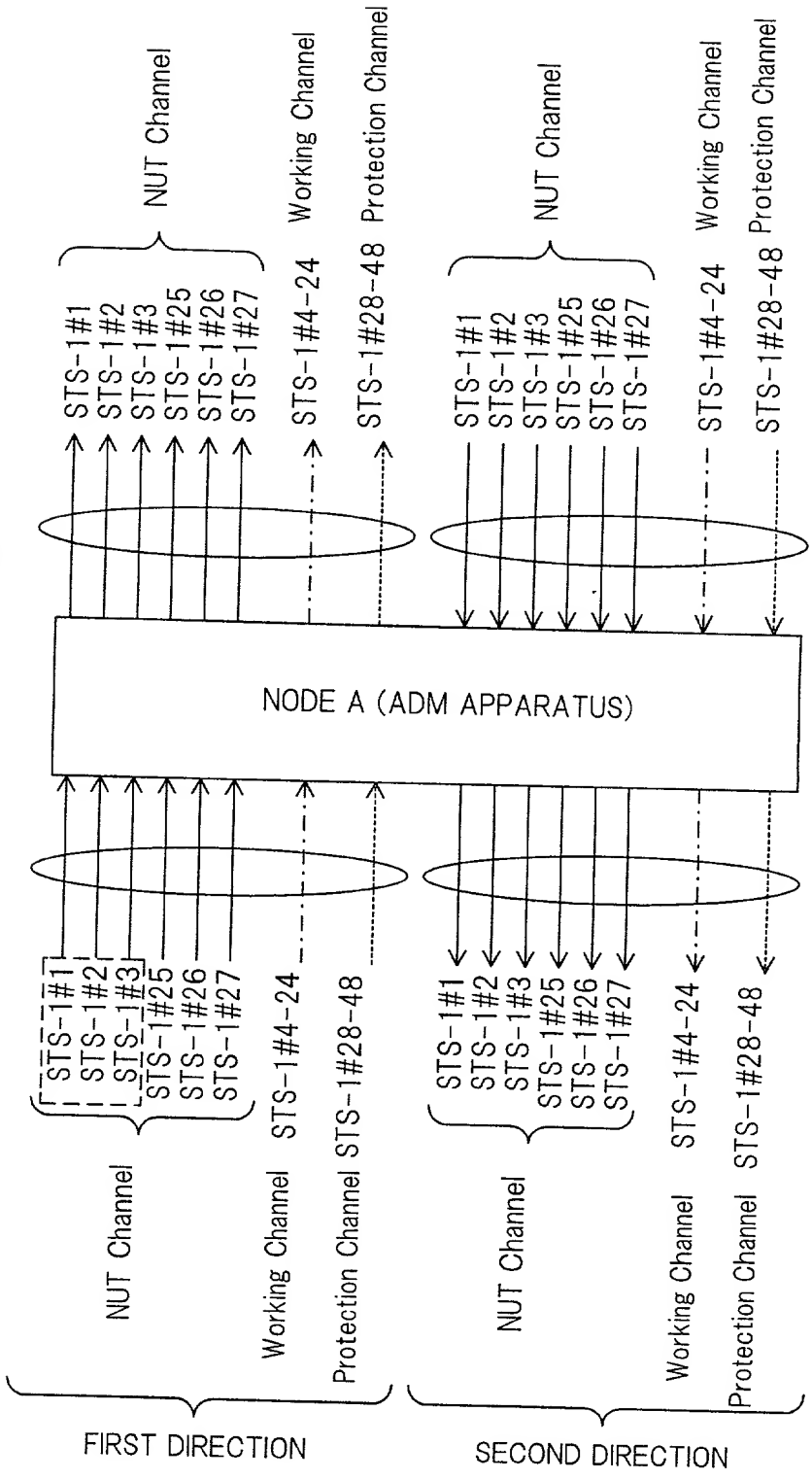
Fiber1(WEST)
Fiber1(East)
NODE A (ADM APPARATUS)
Fiber2
Fiber2
NUT Channel
STS-1#1
STS-1#2
STS-1#3
STS-1#25
STS-1#26
STS-1#27
Working Channel
STS-1#4-24
Protection Channel
STS-1#28-48
FIRST DIRECTION
SECOND DIRECTION

FIG. 5

OC-12 BLSR #1

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	ch6	ch5	ch4	ch3	ch2	ch1

OC-12 BLSR #2

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	*	*	*	ch6	ch5	ch4	ch3	ch2	ch1

OC-48 BLSR

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	ch12	ch11	ch10	ch9	ch8	ch7	ch6	ch5	ch4	ch3	ch2	ch1

OC-48 BLSR

D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
*	*	*	*	ch24	ch23	ch22	ch21	ch20	ch19	ch18	ch17	ch16	ch15	ch14	ch13

"1"=NUT channel
"0"=not NUT channel

FIG. 6

BLSR Type		
OC12-2	OC12-1	OC-48

OC-48: OC-48 BLSR DESIGNATION; "1" : WHEN OC- 48 BLSR; "0" : NOT OC-48 BLSR
OC-12-1: OC-12 BLSR #1 DESIGNATION; "1" : WHEN OC-12 BLSR #1; "0" : NOT OC-12 BLSR #1
OC-12-2: OC-12 BLSR #2 DESIGNATION; "1": WHEN OC-12 BLSR #2; "0" : NOT OC-12 BLSR #2

FIG. 7A

APPLICATION	NUMBER OF NUT CHANNEL SETTING REGISTERS ACCORDING TO PRIOR ART (N)	NUMBER OF NUT CHANNEL SETTING REGISTERS ACCORDING TO PRESENT INVENTION (M)
not BLSR	192	0
OC-12 BLSR		6
OC-48 BLSR		24

(WHEN MAXIMUM VT ACCESS PROCESSING CAPACITY OF APPARATUS IS 10 Gbps)

FIG. 7B

APPLICATION	NUMBER OF BLSR-TYPE SETTING REGISTERS ACCORDING TO PRIOR ART (N)	NUMBER OF BLSR-TYPE SETTING REGISTERS ACCORDING TO PRIOR ART (L)
WHEN OC-12 BLSR, OC-48 BLSR OR ITEM OTHER THAN BLSR CAN BE SELECTED	192	2

(WHEN MAXIMUM VT ACCESS PROCESSING CAPACITY OF APPARATUS IS 10 Gbps)

FIG. 7C

APPLICATION	NUMBER OF SQL ACTIVATE PROCESSING CHANNELS ACCORDING TO PRIOR ART (NxVT*)	NUMBER OF SQL ACTIVATE PROCESSING CHANNELS ACCORDING TO PRESENT INVENTION (MxVT*)
not BLSR	5376	0
OC-12 BLSR		168 (=6×28)
OC-48 BLSR		672 (=24×28)

(WHEN MAXIMUM VT ACCESS PROCESSING CAPACITY OF APPARATUS IS 10 Gbps)

FIG. 8

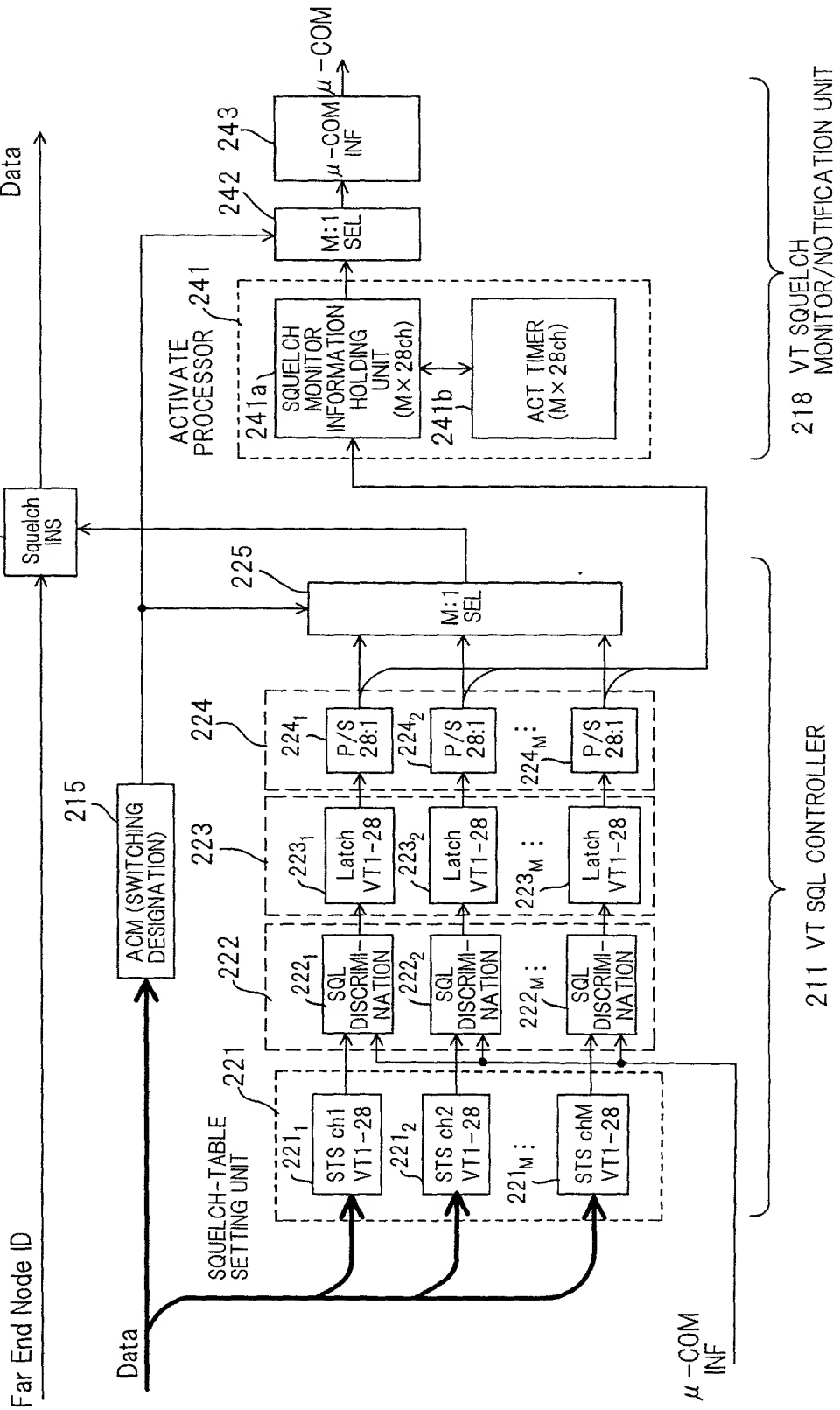
Far End Node ID
Data
Data
μ-COM INF
SQUELCH-TABLE SETTING UNIT
221
221_1 STS ch1 VT1-28
221_2 STS ch2 VT1-28
221_M STS chM VT1-28
222
222_1 SQL DISCRIMI-NATION
222_2 SQL DISCRIMI-NATION
222_M SQL DISCRIMI-NATION
223
223_1 Latch VT1-28
223_2 Latch VT1-28
223_M Latch VT1-28
224
224_1 P/S 28:1
224_2 P/S 28:1
224_M P/S 28:1
225 M:1 SEL
215 ACM (SWITCHING DESIGNATION)
212 Squelch INS
ACTIVATE PROCESSOR 241
241a SQUELCH MONITOR INFORMATION HOLDING UNIT (M×28ch)
241b ACT TIMER (M×28ch)
242 M:1 SEL
243 μ-COM INF
μ-COM
211 VT SQL CONTROLLER
218 VT SQUELCH MONITOR/NOTIFICATION UNIT

FIG. 9

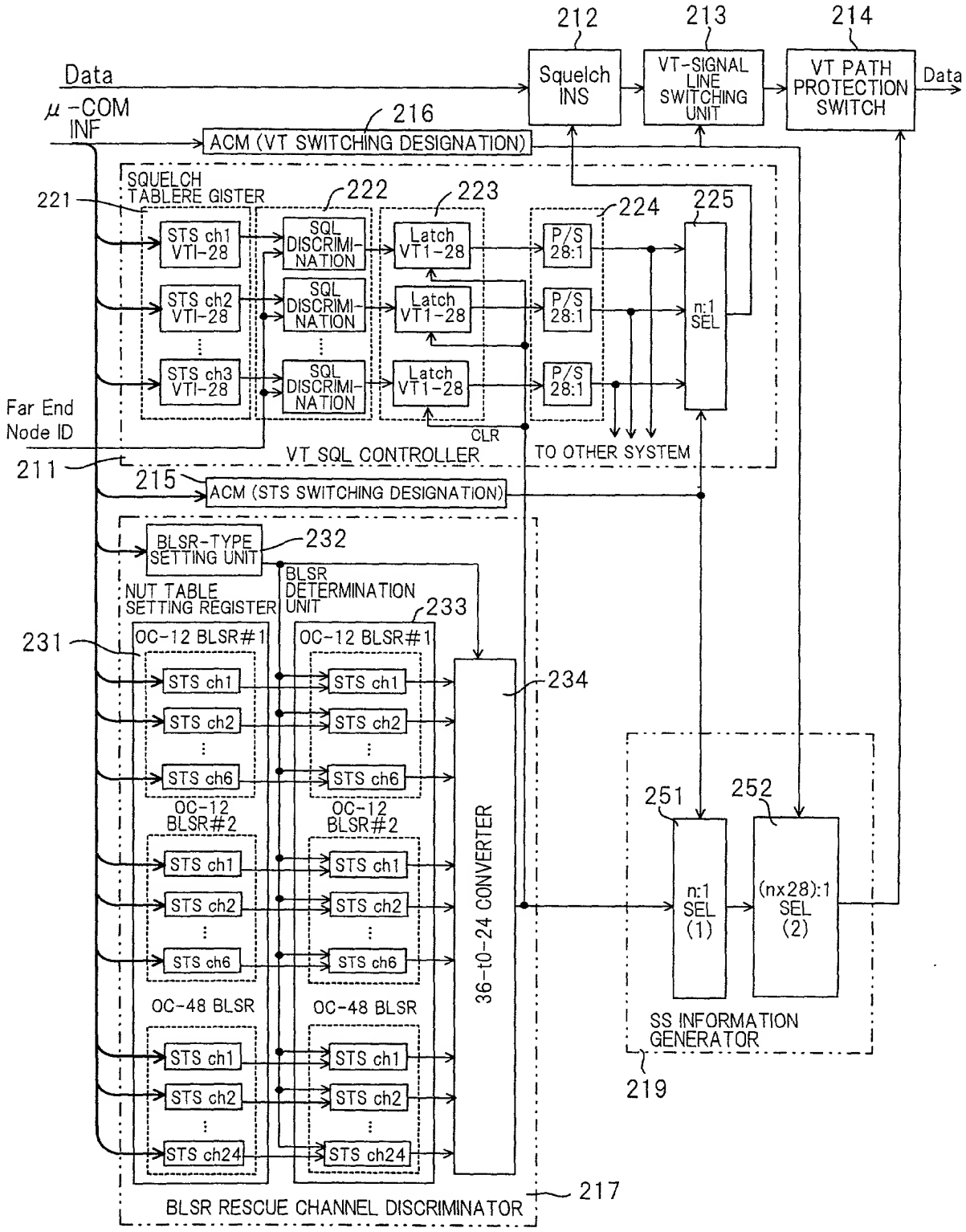
212
213
214
Data
Squelch INS
VT-SIGNAL LINE SWITCHING UNIT
VT PATH PROTECTION SWITCH
Data
μ-COM INF
216
ACM (VT SWITCHING DESIGNATION)
SQUELCH TABLERE GISTER
221
222
223
224
225
STS ch1 VTI-28
STS ch2 VTI-28
STS ch3 VTI-28
SQL DISCRIMI-NATION
Latch VT1-28
P/S 28:1
n:1 SEL
Far End Node ID
CLR
VT SQL CONTROLLER
TO OTHER SYSTEM
211
215
ACM (STS SWITCHING DESIGNATION)
BLSR-TYPE SETTING UNIT
232
BLSR DETERMINATION UNIT
NUT TABLE SETTING REGISTER
233
231
OC-12 BLSR#1
OC-12 BLSR#2
OC-48 BLSR
STS ch1
STS ch2
STS ch6
STS ch24
234
36-t0-24 CONVERTER
251
252
n:1 SEL (1)
(nx28):1 SEL (2)
SS INFORMATION GENERATOR
219
BLSR RESCUE CHANNEL DISCRIMINATOR
217

FIG. 10

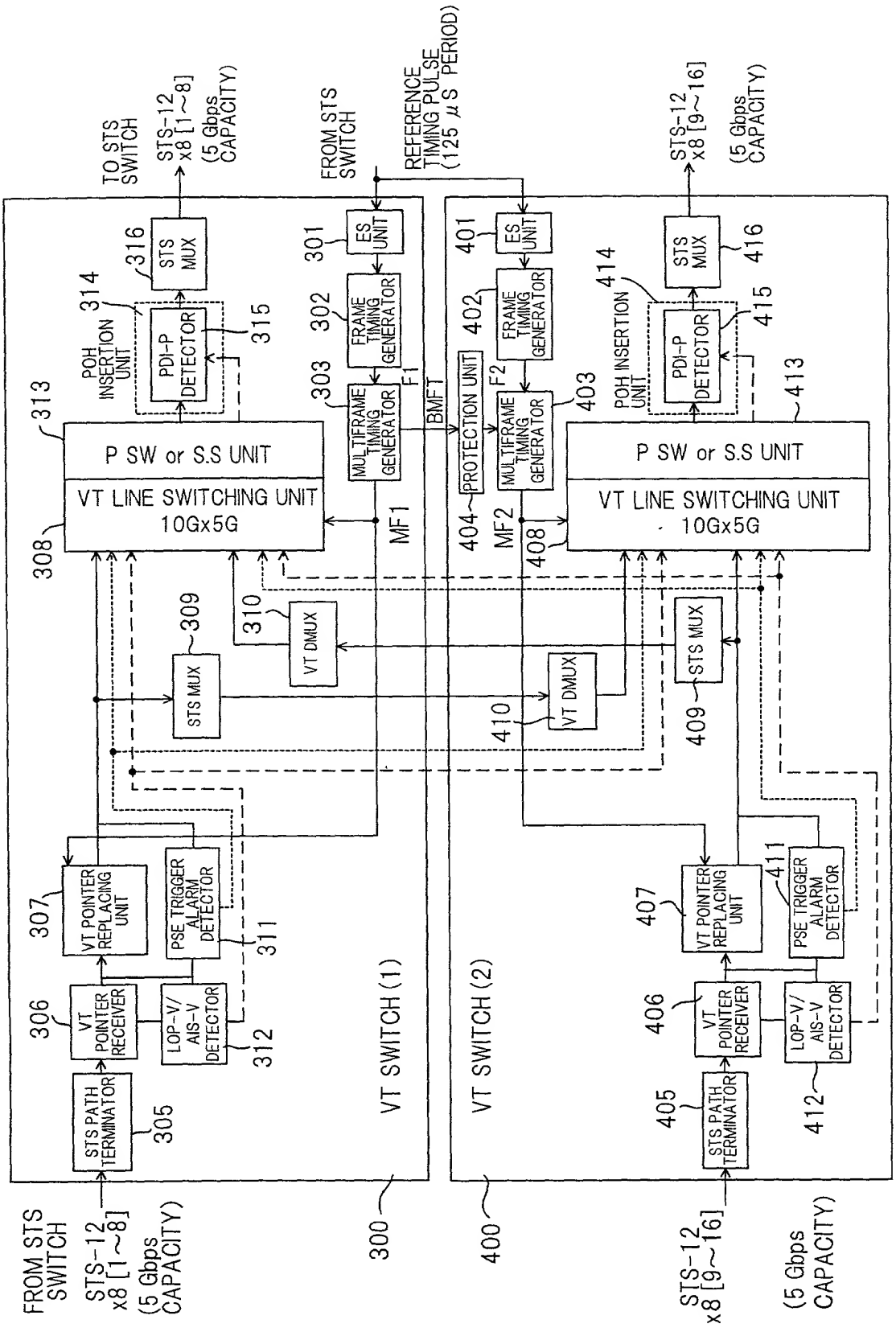
FROM STS SWITCH
STS-12 x8 [1~8]
(5 Gbps CAPACITY)
STS-12 x8 [9~16]
(5 Gbps CAPACITY)
TO STS SWITCH
STS-12 x8 [1~8]
(5 Gbps CAPACITY)
FROM STS SWITCH
REFERENCE TIMING PULSE (125 μS PERIOD)
STS-12 x8 [9~16]
(5 Gbps CAPACITY)
300
VT SWITCH (1)
400
VT SWITCH (2)
P SW or S.S UNIT
VT LINE SWITCHING UNIT 10Gx5G
STS PATH TERMINATOR
VT POINTER RECEIVER
LOP-V/ AIS-V DETECTOR
VT POINTER REPLACING UNIT
PSE TRIGGER ALARM DETECTOR
STS MUX
VT DMUX
POH INSERTION UNIT
PDI-P DETECTOR
ES UNIT
FRAME TIMING GENERATOR
MULTIFRAME TIMING GENERATOR
PROTECTION UNIT
BMFT
MF1
MF2
F1
F2
301
302
303
307
308
309
310
311
312
313
314
315
316
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416

FIG. 11

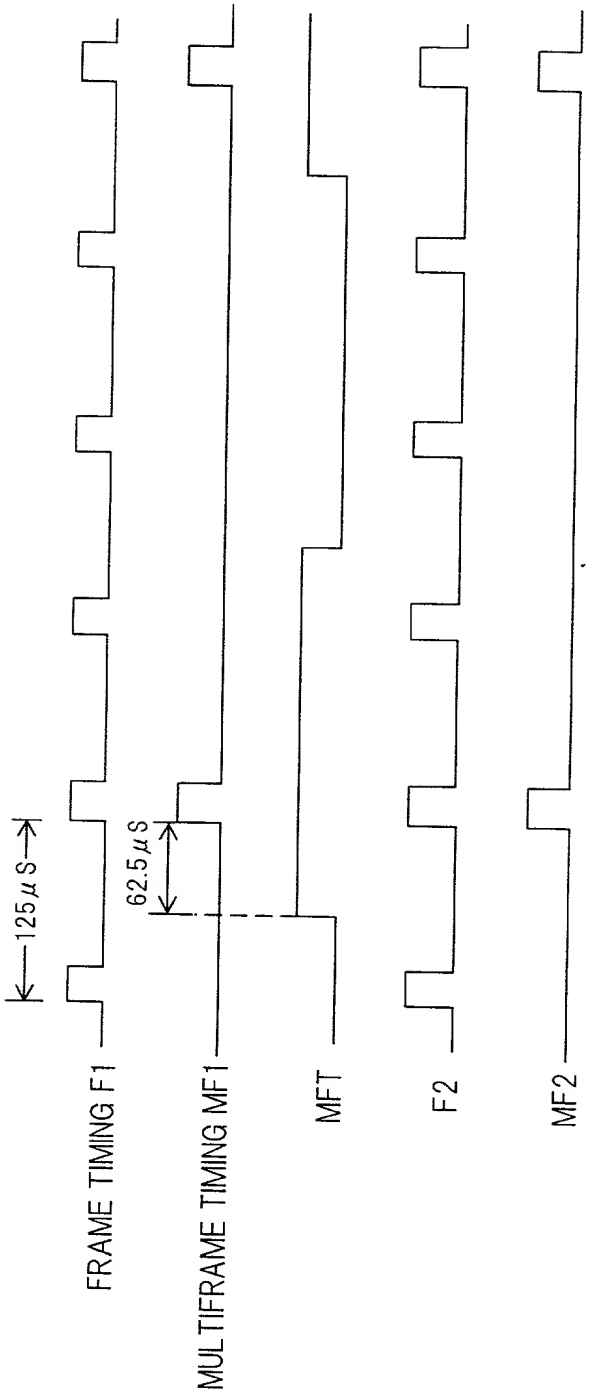
125μS
62.5μS
FRAME TIMING F1
MULTIFRAME TIMING MF1
MFT
F2
MF2

FIG. 12 PRIOR ART

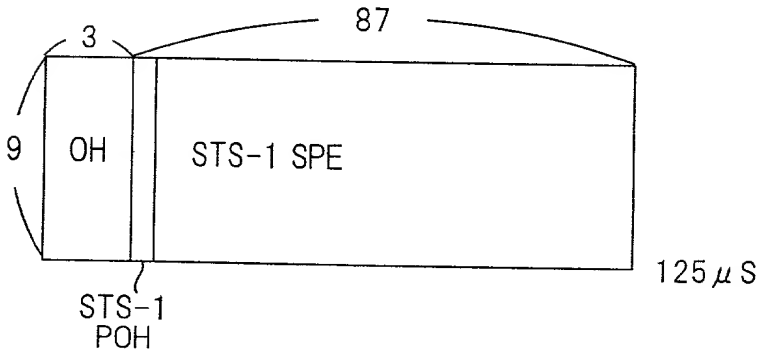

FIG. 13 PRIOR ART

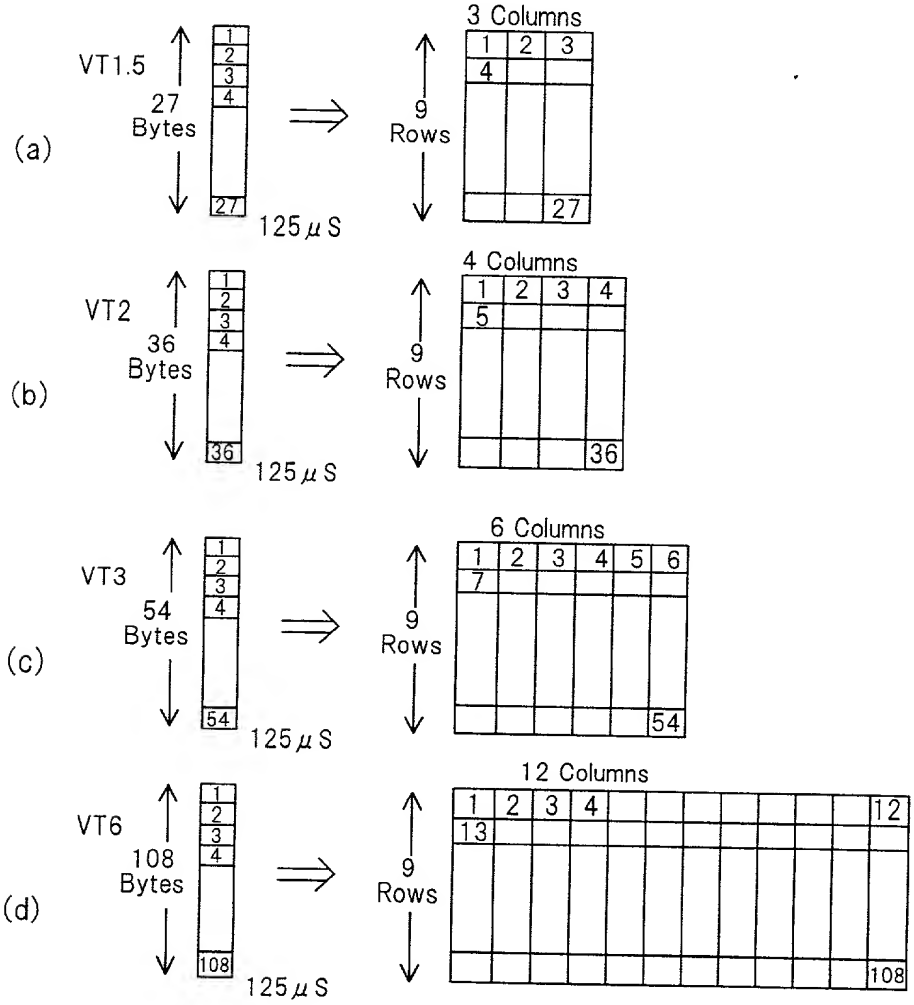

FIG. 14 PRIOR ART

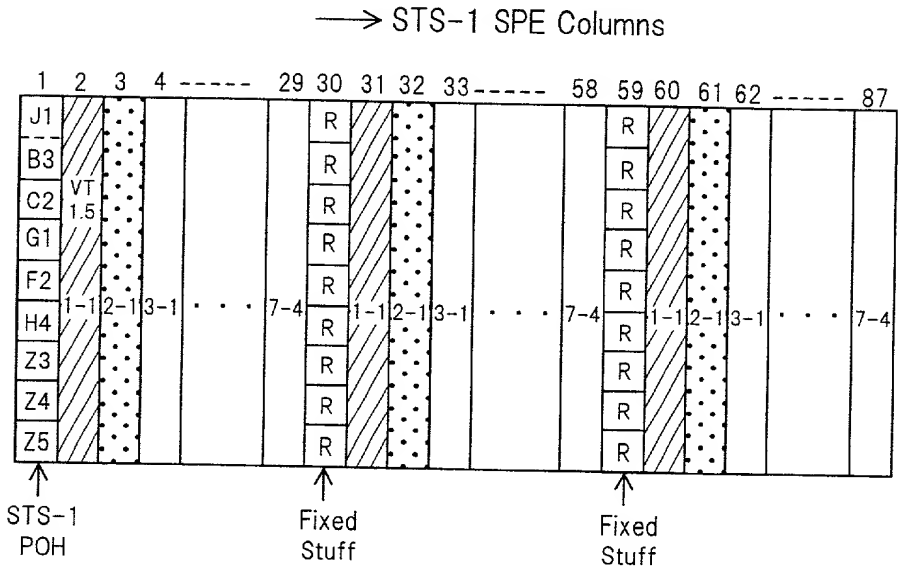

FIG. 15 PRIOR ART

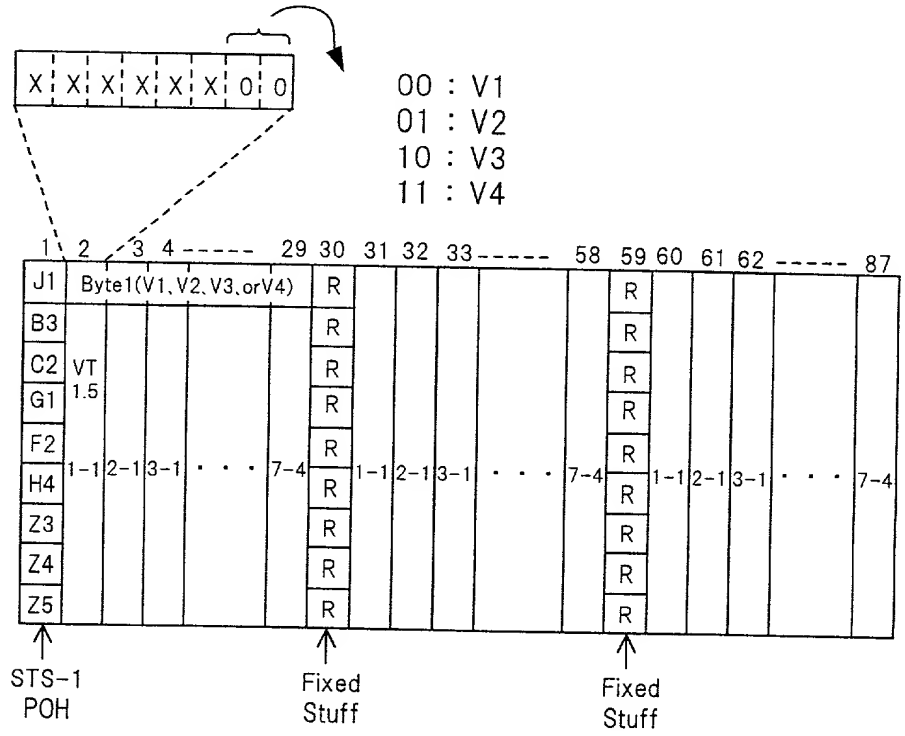

FIG. 16A PRIOR ART

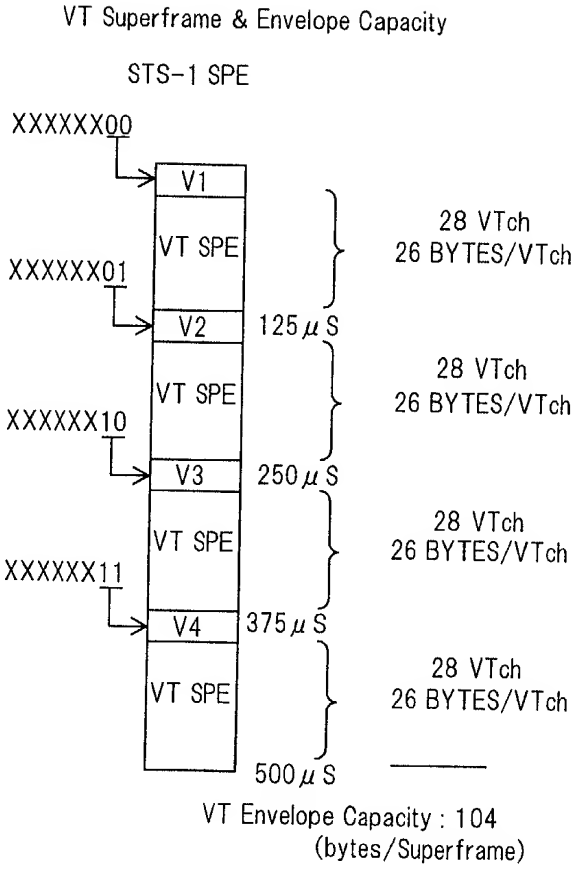

FIG. 16B PRIOR ART

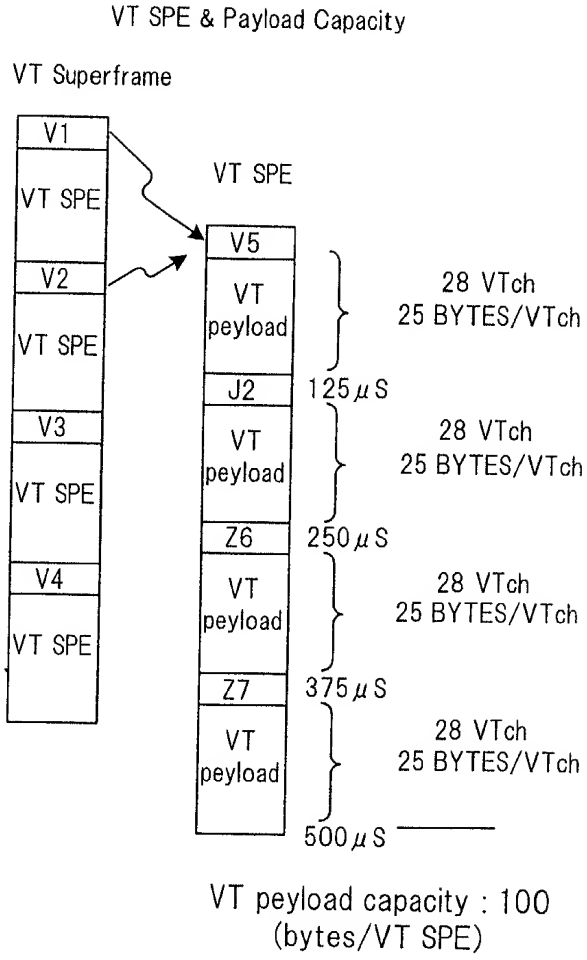

FIG. 17 PRIOR ART

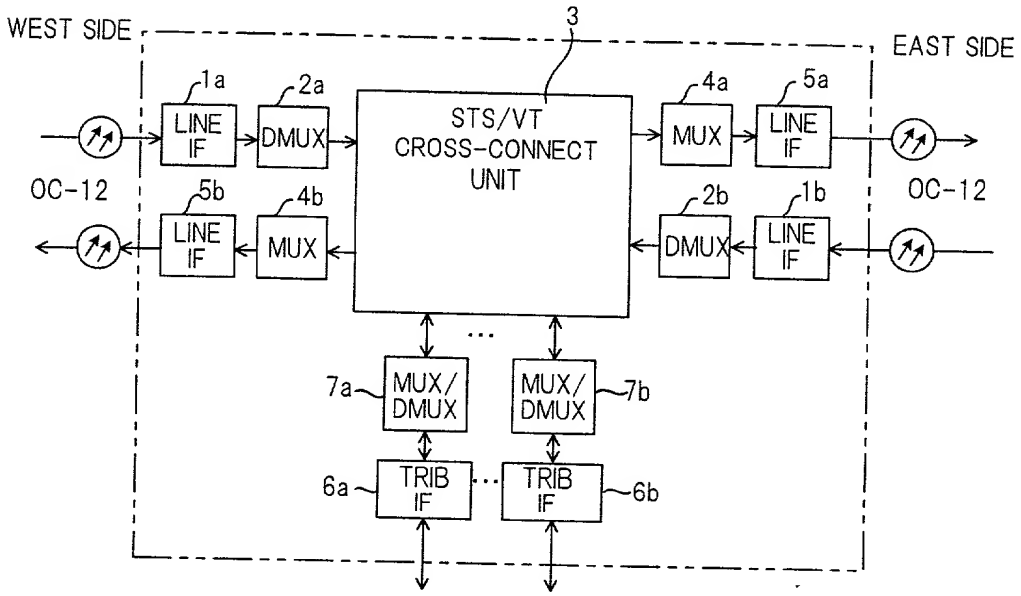

FIG. 18 PRIOR ART

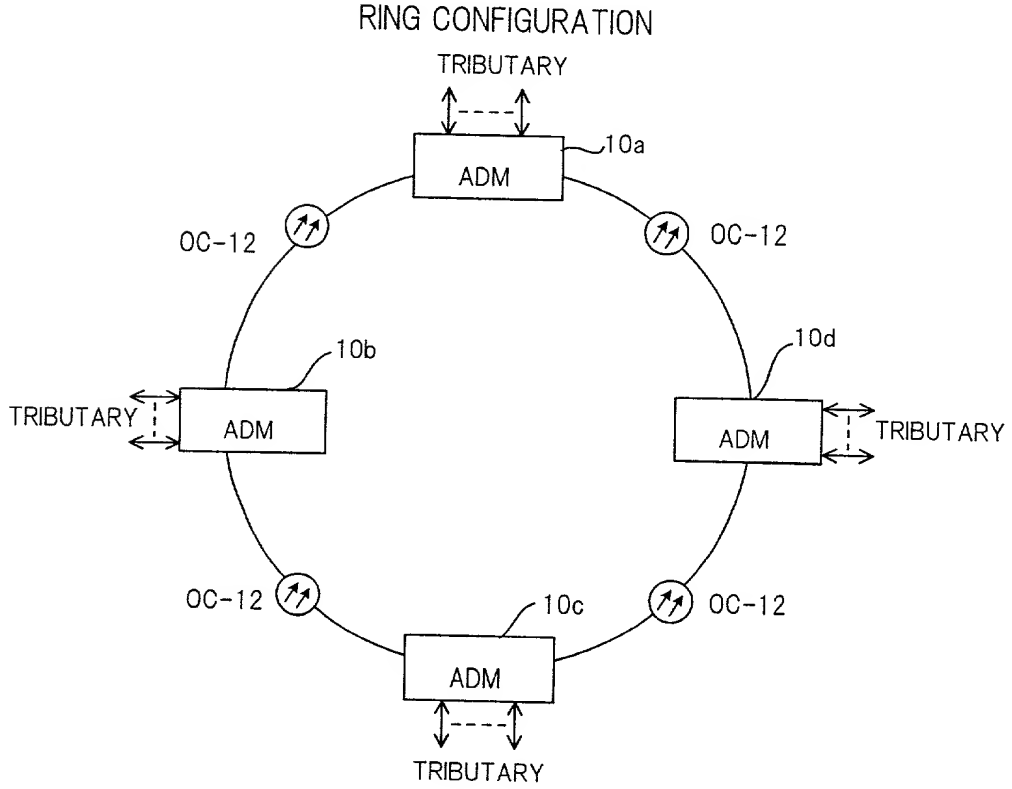

FIG. 19 PRIOR ART

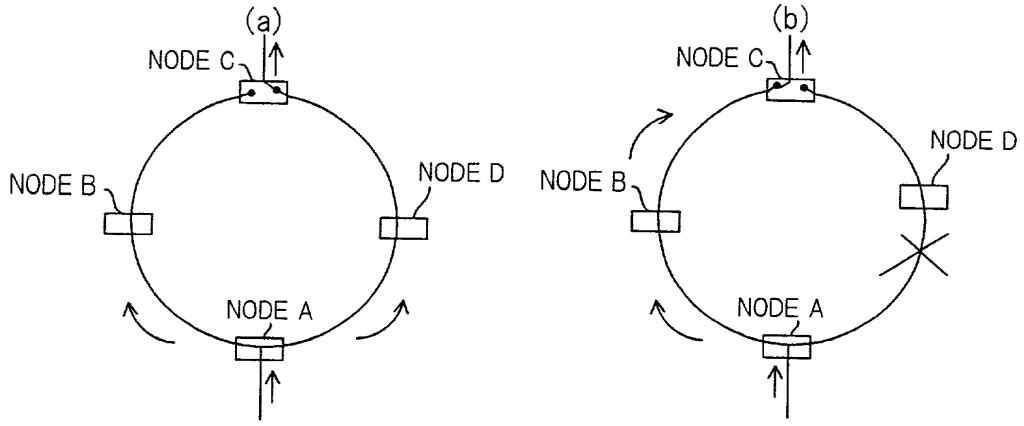

FIG. 20 PRIOR ART

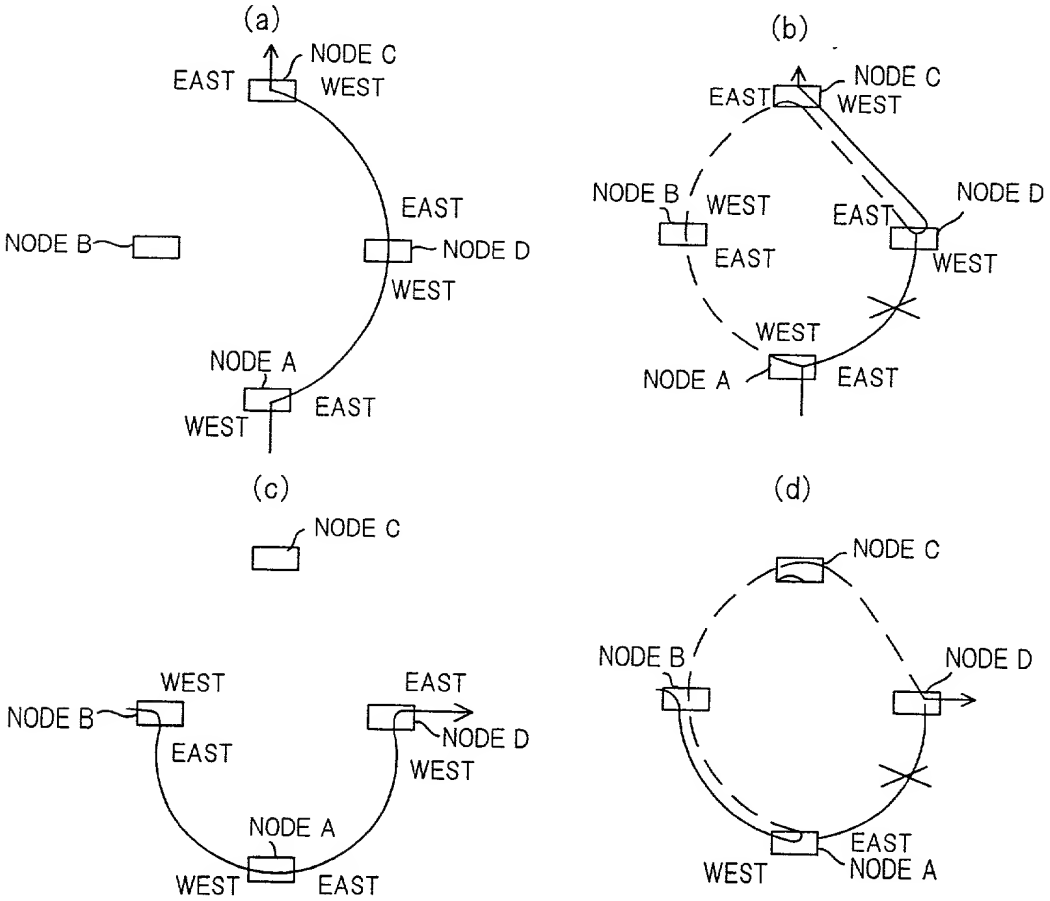

FIG. 21 PRIOR ART

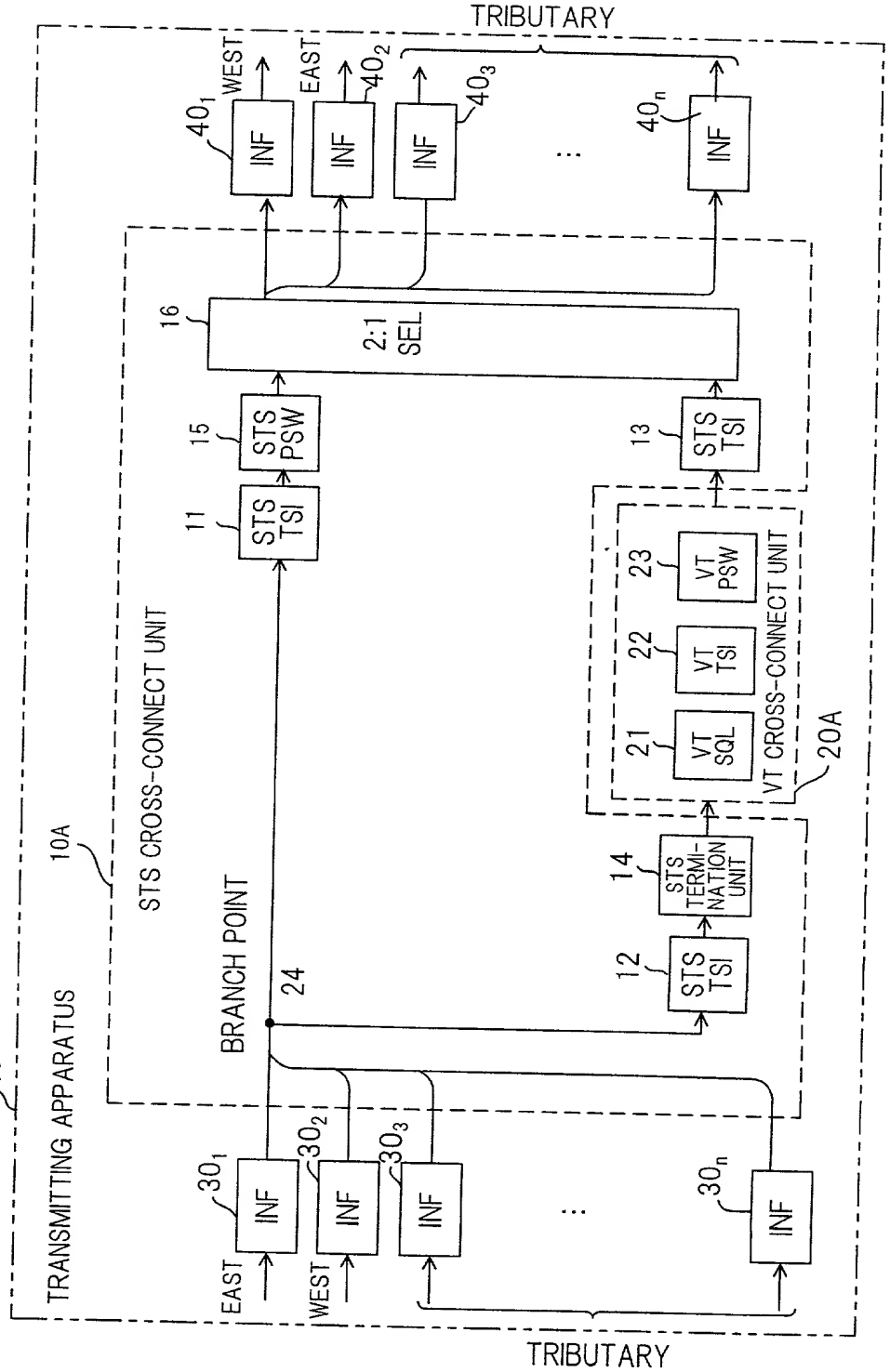

FIG. 22A PRIOR ART

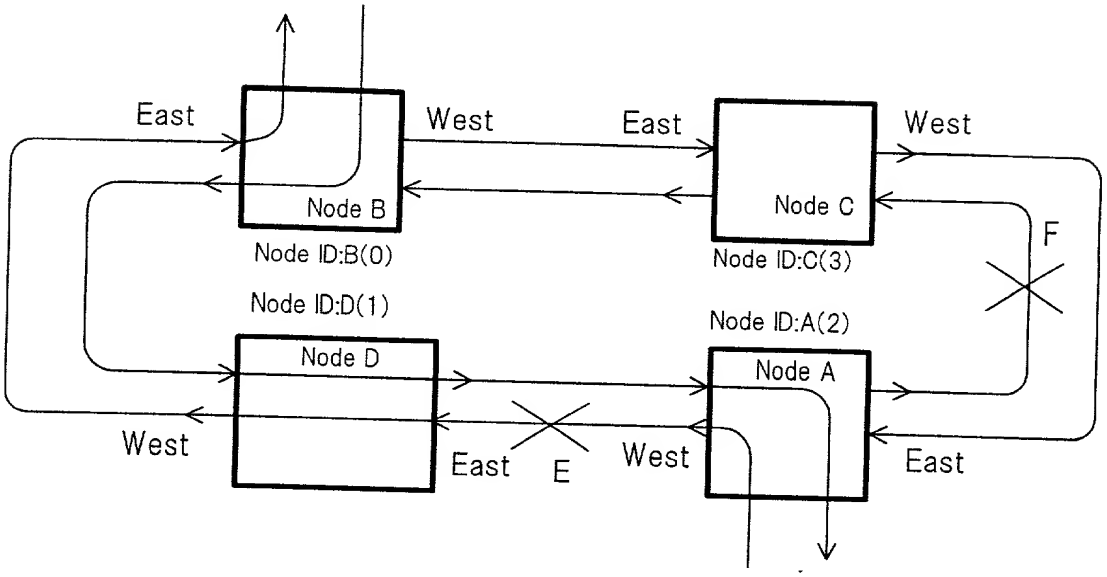

FIG. 22B PRIOR ART

Node B VT Squelch Table

East Side	West Side
2	0

FIG. 23 PRIOR ART

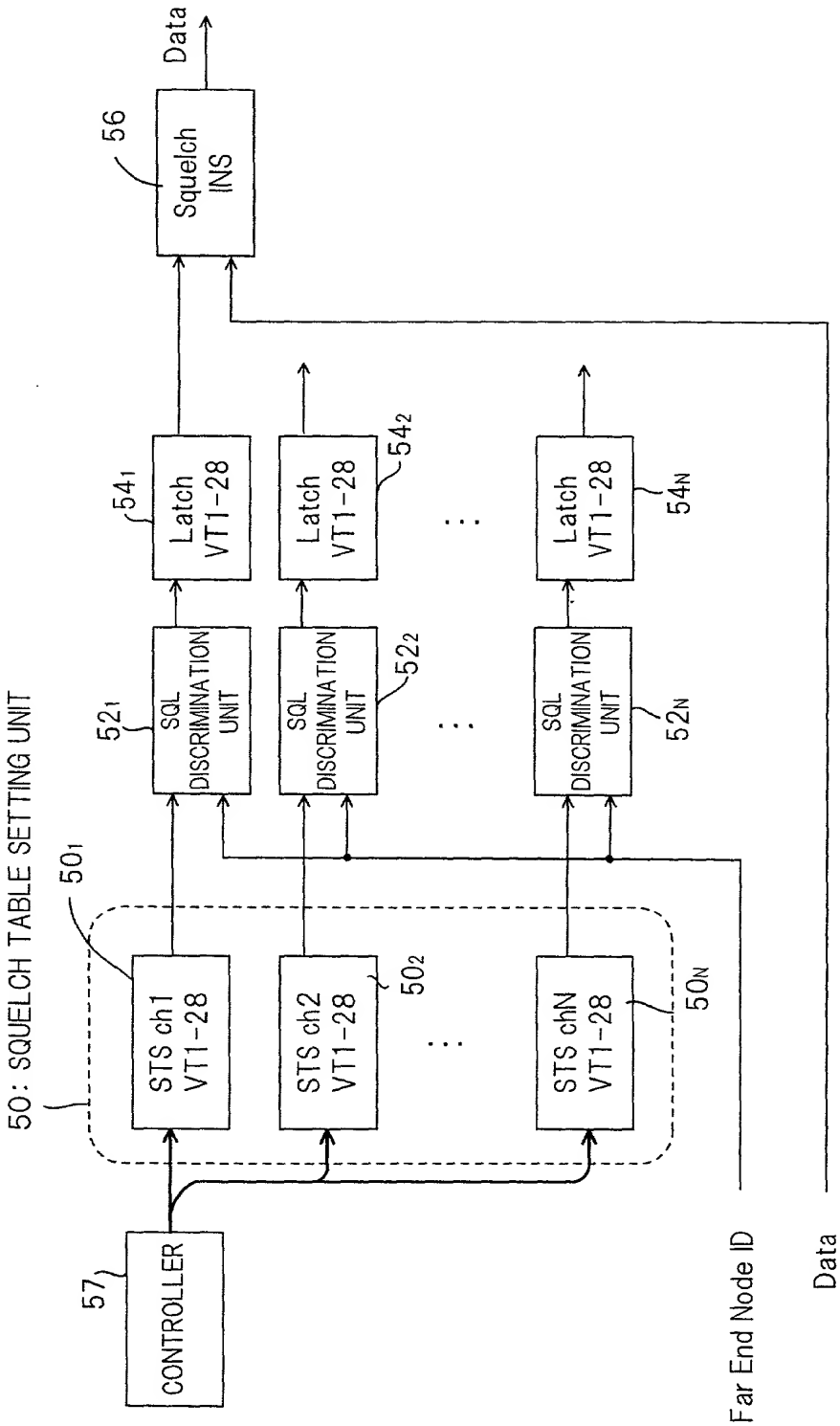

FIG. 24 PRIOR ART

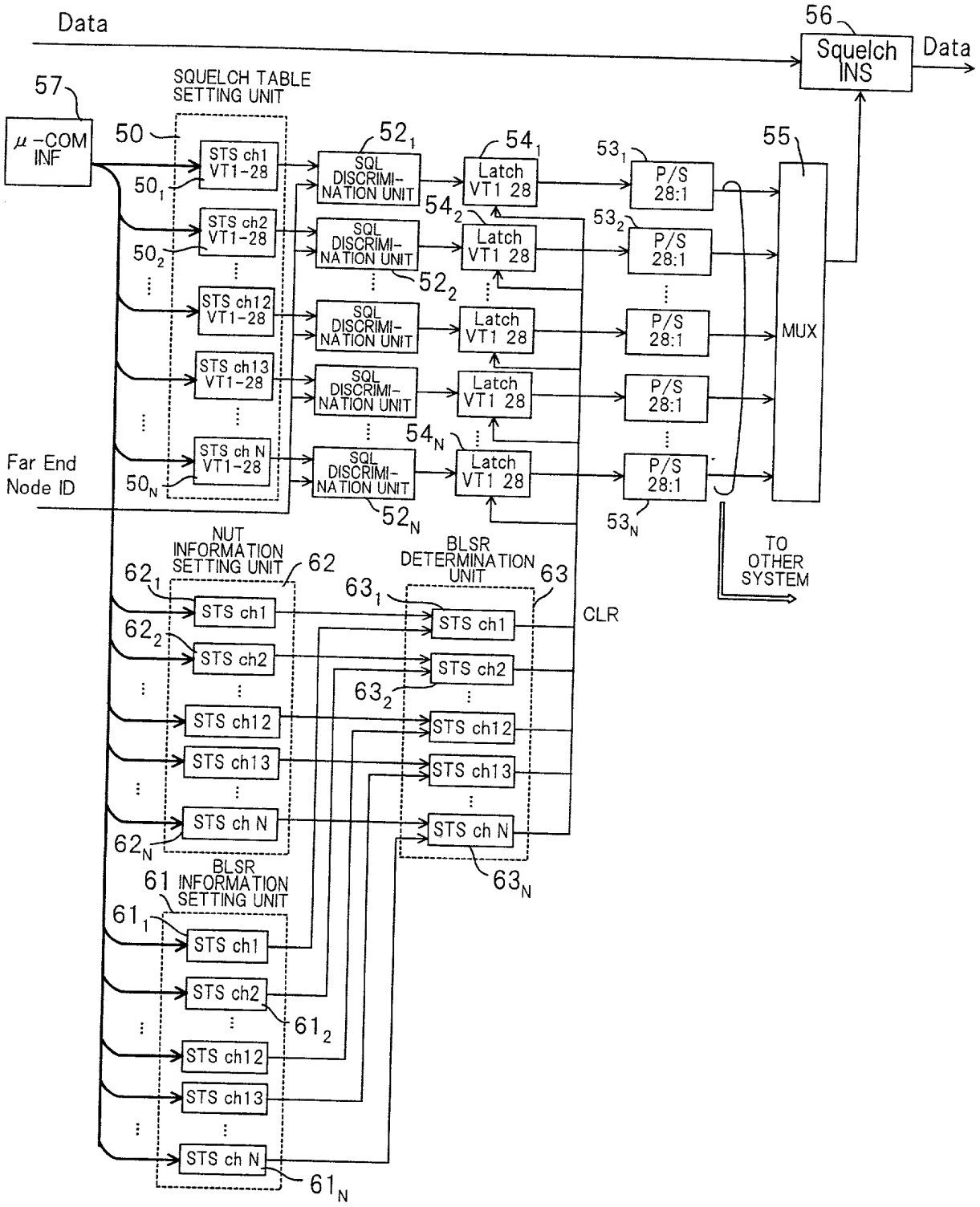

FIG. 25 PRIOR ART

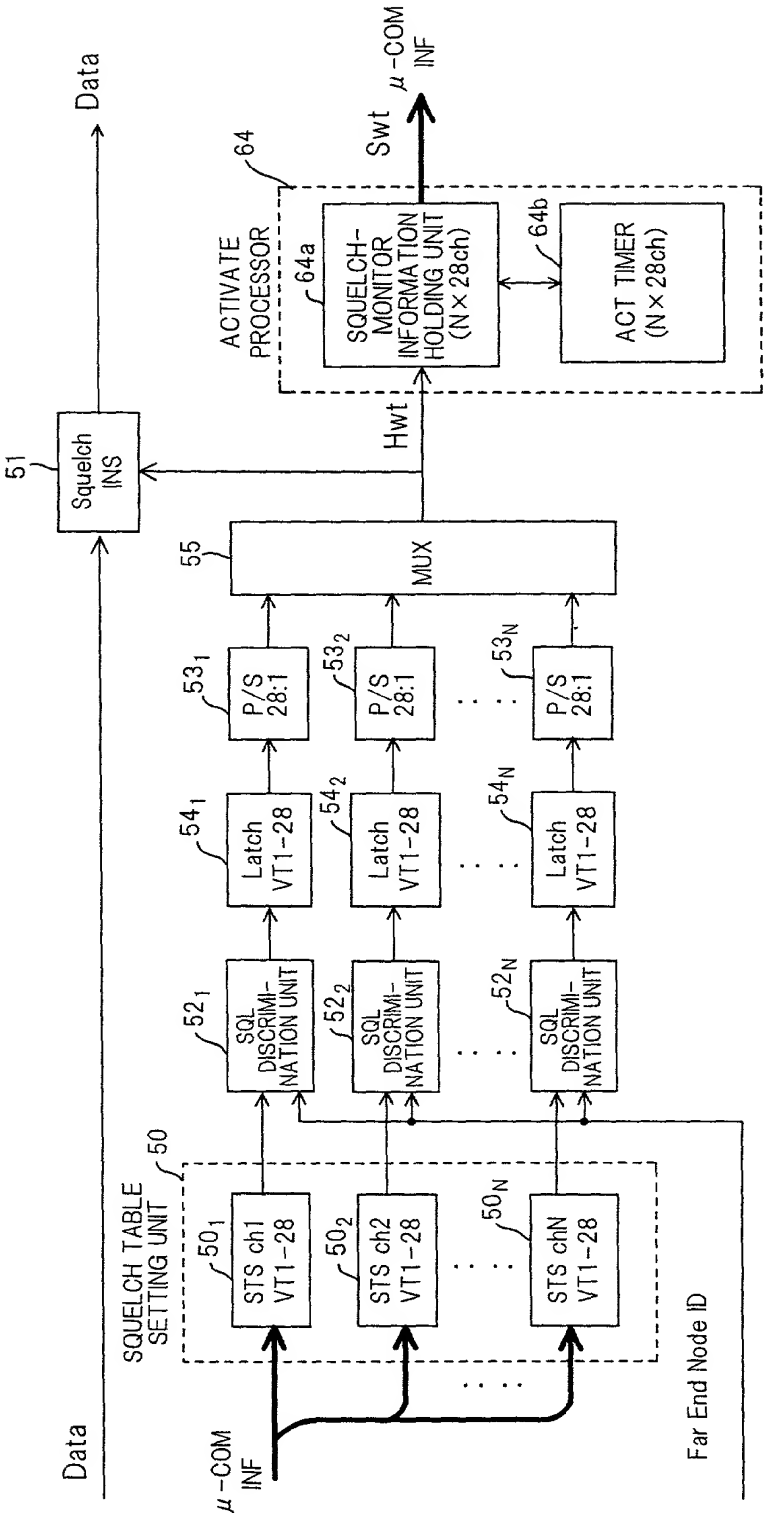

FIG. 26 PRIOR ART

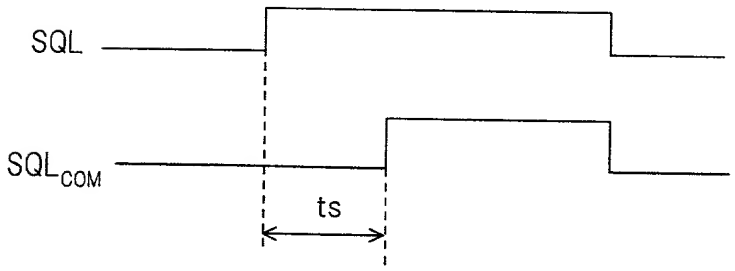

FIG. 27 PRIOR ART

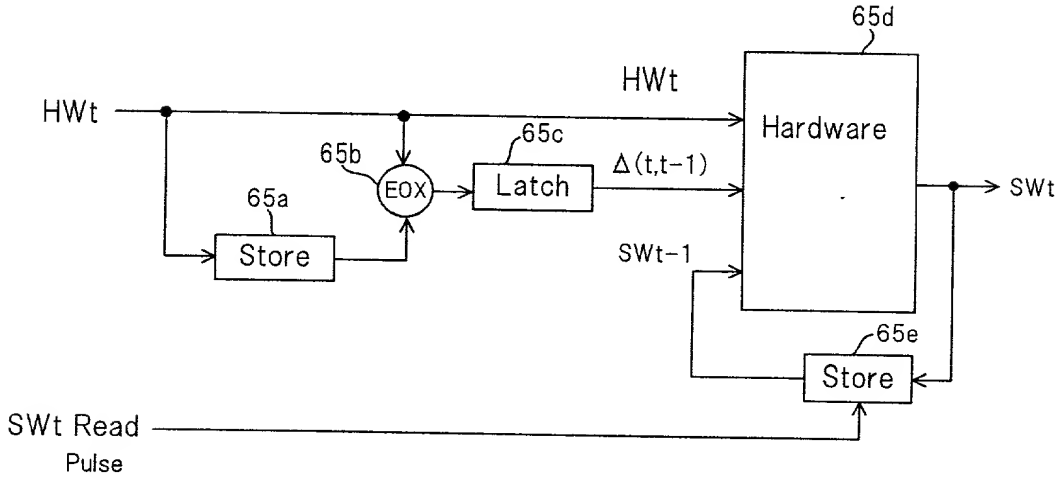

FIG. 28 PRIOR ART

SWt-1	Δ(t,t-1)	HWt	SWt
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

FIG. 29 PRIOR ART

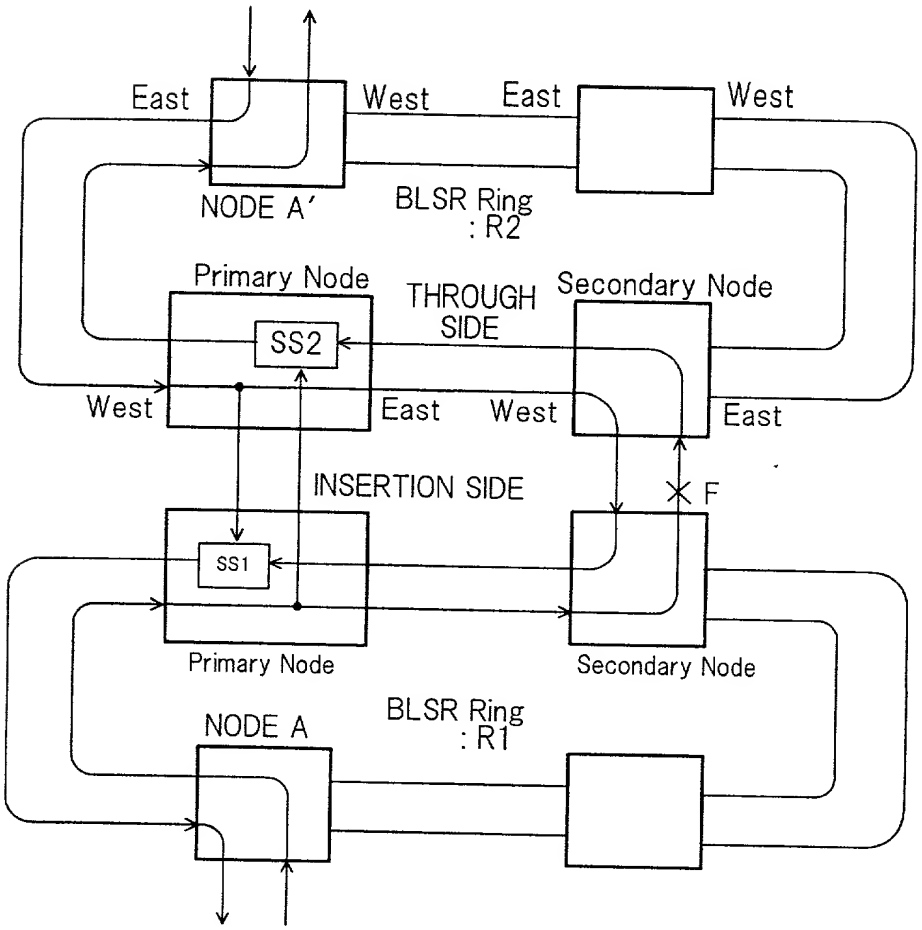

FIG. 30 PRIOR ART

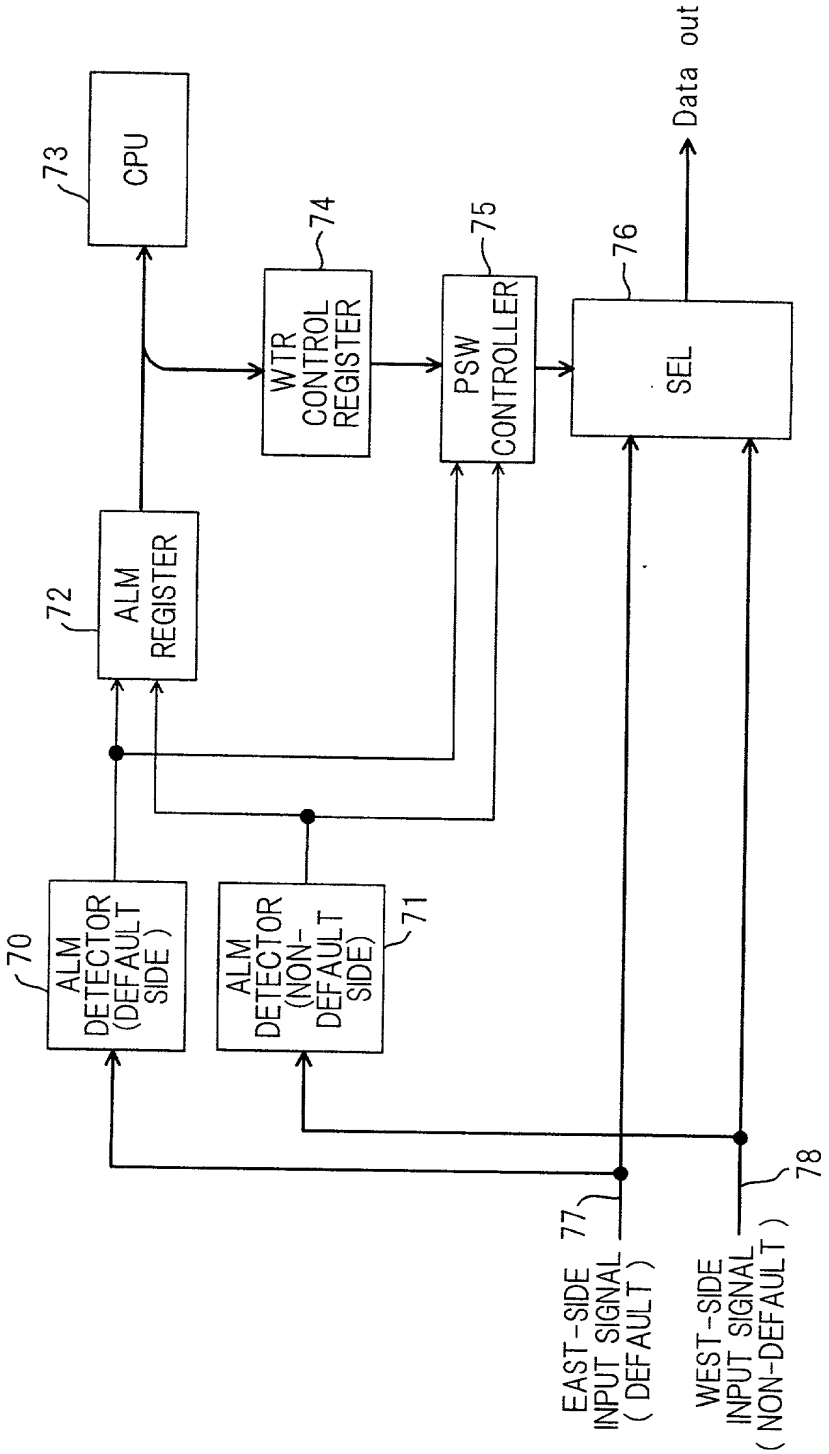

FIG. 31 PRIOR ART

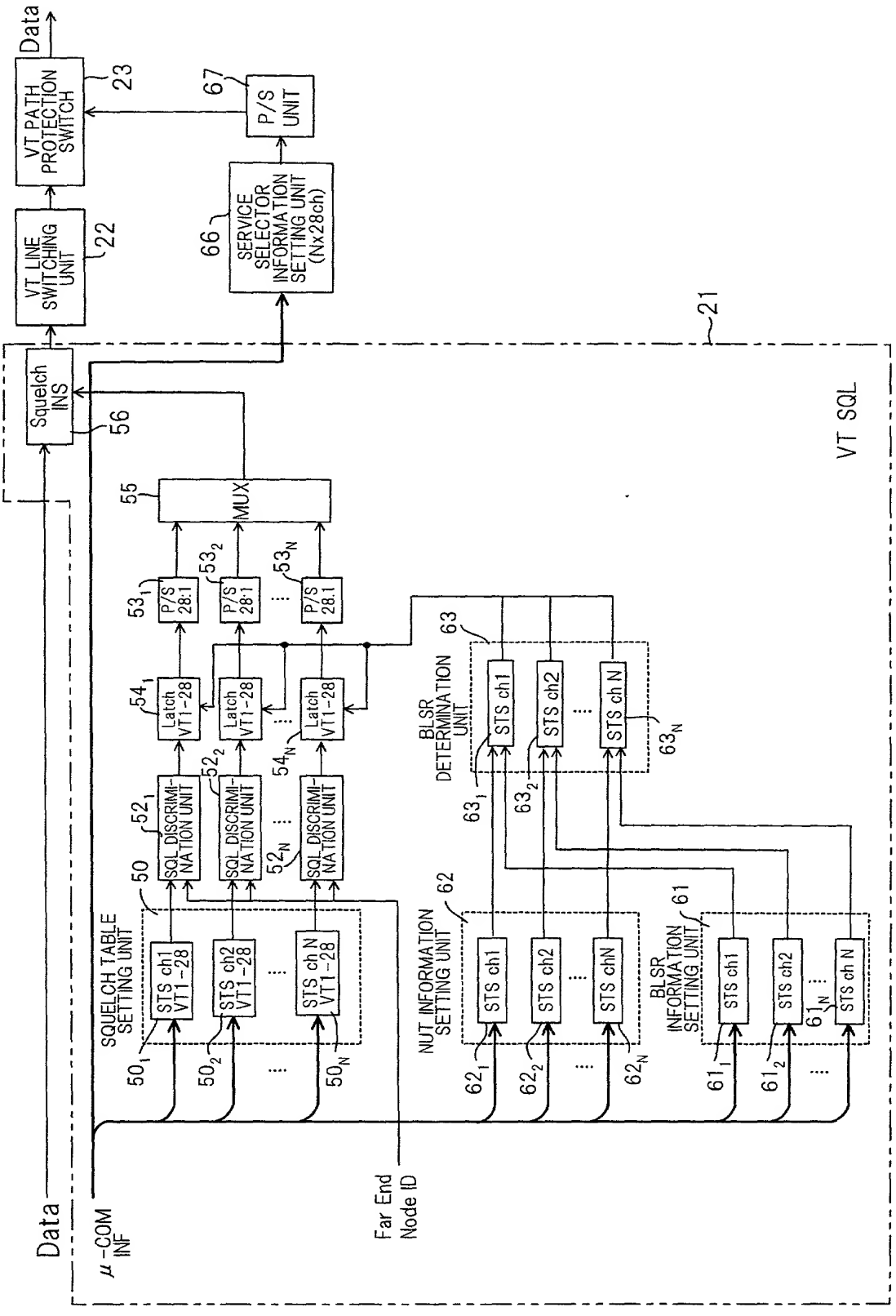

FIG. 32 PRIOR ART